High Performance Control Design for Dynamic Voltage Scaling Devices

Carolina Albea-Sanchez, Francisco Gordillo Álvarez, Carlos Canudas de Wit

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***Abstract*—Dynamic Voltage Scaling (DVS) is an important method in managing dynamically the system supply voltage for efficient power reduction. This approach is applied in Very-Large-Scale Integration (VLSI). A DC-DC converter is an electronic device which allows to vary the voltage and, thus, to implement DVS technique.**

In this paper, a high-performance controller is presented for a novel discrete DVS converter. This controller is developed with the aim to deal with the unknown resistive component of the load as well as to minimize the dissipated energy and current peaks, what is very important in the field of microelectronics. Current peaks and power consumption are minimized by computing an optimal evolution for the voltage reference. Likewise, an adaptive controller is proposed to deal with the unknown load resistive parameter. Consequently, the obtained advanced controller can acquires a high consideration on electronic devices.

***Index Terms*—Dynamic voltage scaling, energy aware, Lyapunov's methods, optimal control, adaptive control**

I. Introduction

The development of low-power electronic devices has raised up in recent years. Very-Large-Scale Integration (VLSI) is mostly used in information technology-related products, such as PCs, mobile devices and digital consumer equipments.

Dynamic Voltage Scaling (DVS) is a known technique that adjusts the processor voltage supply to the minimum level of performance required by the system application [1], [2]. DC-DC converters are a key element in a DVS mechanism, since they can dynamically adapt the supply voltage. This technology has been employed in VLSI. However, this kind of converters has a different structure than the standard ones since they must change the operating voltage in a dynamic way [3], [4]. Likewise, the controllers of these DC-DC converters present a relevant interest [5].

A dynamic continuous buck converter for DVS systems was presented in [6], which provides suited performance. It, however, limits SoC scaling properties due to the size of the inductive component. In the framework of SoC miniaturization, a discrete DC-DC converter was developed in [7]. It is composed of two supply sources and a Power Supply Selector (PSS). This discrete DVS converter replaces the inductive element with a set of CMOS transistors, reducing the converter required size.

Control objective for the discrete DVS converter is to achieve the target voltage providing a correct and reliable operation during the switching transitions. Therefore, the control must achieve:

- small current peaks,
- fast transient periods,
- minimum dissipated energy,
- adaptation to unknown load and
- low performance cost.

A simple discrete controller was proposed in [7] to handle the two-voltage level required for the discrete DVS converter. In this control structure, only one transistor can be switched at each sampling time. This limits the ability of the converter to make fast transient periods. In addition, the employed voltage reference was a ramp with a computed slope to obtain small current peaks.

In the first part of this paper, a high-performance control law for discrete DVS converter is developed, without the constraint that only one transistor can be switched at each sampling time. [8]. This allows to obtain a richer control sequence and, thus, better expected performance with respect to the issues previously mentioned. The controller is based on Lyapunov theory, being developed in order to improve the tracking capability and their regulation characteristic. As a side effect, it is also observed that the current peaks are reduced during the transient periods.

This controller is compared with the controller proposed in [7] in terms of: transient response, quality of the induced load current, power consumption and performance cost. The high-performance controller presents suited properties. Nevertheless, it needs knowledge of the load and, current peaks and energy-saving are not necessarily optimal. These important issues are also dealt with in this work.

In the second part of this paper the Lyapunov-based controller is improved in two directions: on the one hand, optimal control theory is applied in order to achieve minimum current peaks and maximum energy efficiency. For this purpose, an optimal evolution for the voltage reference is obtained by solving a Boundary Value Problem (BVP) with transversality condition. This problem is numerically solved by using the MATLAB function bvp4c [9], [7].

On the other hand, an adaptation mechanism is added to the Lyapunov-based control law in order to cope with load uncertainties. Modelling the load connected to the

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discrete DVS converter is involved. In some occasions, it is designed as a dynamic resistance modeled as function depending on the voltage and chip frequency [10], [11], among other components. However, this is not an accurate model. This is why this resistance connected to the DVS converter should be considered unknown or/and slowly changing. For this reason, an adaptive strategy is implemented in such a way that the load resistive component is adapted.

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The rest of this work is organized as follows: in Section II, the circuit model of the discrete DVS converter is presented as well as their properties and the error equation. A high-performance controller for the discrete DVS converter is proposed in Section III, explaining in Section IV its implementation. Next up, a performance evaluation of the controller is done in Section V. Section VI states the possibility to improve the high-performance controller by employing optimal and adaptive control. They are developed in Section VII (optimal control) and VIII (adaptive law). A performance evaluation of this advanced controller is presented in Section IX. The work closes with a section of conclusions.

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Notation. Denote:

$$\mathrm{sat}_m^M(x) = \begin{cases} M & \text{if} \quad x > M \\ x & \text{if} \quad m \le x \le M \\ m & \text{if} \quad x < m. \end{cases},$$

round(x) is the nearest integer to x, and q^{-1} is the discrete-time parameter, i.e. $x_{k-1} = q^{-1}x_k$.

II. Model of a discrete DVS converter

A discrete DVS converter handling two-voltage levels with a PSS structure was proposed in [7]. Its main advantage is the possibility to reduce the SoC scale because it does not need passive components. It is composed of a PSS and two external supply voltages. A high voltage supply, V_h, for a unit running at nominal speed and a low voltage supply, V_l, for a unit running at reduced speed. Its structure is shown in Fig. 1.

A PSS is constituted by a group of PMOS transistors connected in parallel with common drain, source and bulk but separated gates in order to scale the output voltage from V_h to V_l and vice-versa. On the other side, v_c is the output core voltage of the system. The PMOS transistor that connects the V_l to the voltage output v_c is switched on when V_l is the selected power supply. This reduces the dissipated energy when the unit running is at low speed. Other component in the PSS is a control block that provides a control signal u_k for the PMOS transistors. Besides it generates a reference signal v_r. Likewise, this control block has as inputs: a clock signal (CLK), a local power manager signal (LPM), that orders to the PSS to start the hopping sequence and an error voltage signal, e, from a comparator.

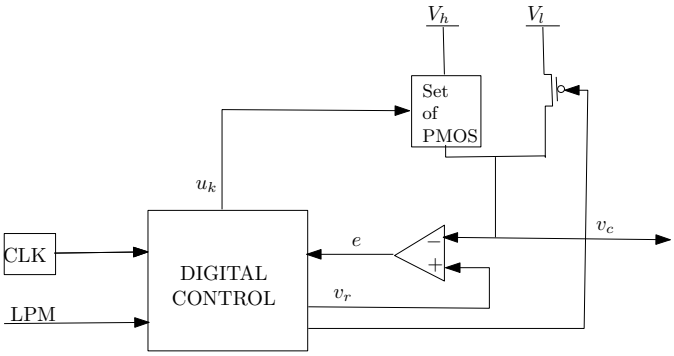

Fig. 1: DVS converter.

Load model.

The discrete DVS converter is connected to a load that can be modeled as an impedance depending on the core voltage, v_c. In this work, the load model implemented in VHDL-AMS in [12] is employed:

$$I_l = f(v_c) = I_{dyn} + I_{short} + I_{leak} + I_{cap} \quad (1)$$

$$I_{dyn} = K_{dyn}\omega v_c \quad (2)$$

$$I_{short} = K_{short}\omega(v_c - 2V_{th})^3 \quad (3)$$

$$I_{leak} = K_{leak} \quad (4)$$

$$I_{cap} = C\frac{dv_c}{dt}, \quad (5)$$

where C, K_{dyn}, K_{short} and K_{leak} depend on the real consumption estimations. V_{th} is the threshold voltage, which must fulfill $v_c > 2V_{th}$. Likewise, the impedance frequency is modelled[2]

$$\omega \triangleq \omega_n(1.735 - 6.746v_c + 7.872v_c^2 - 2.299v_c^3). \quad (6)$$

ω_n is the system frequency.

Figure 2 shows the representation of the load model used in this research. r_L contains the dynamic resistance. For simplicity reasons, firstly, a constant average value of r_L is taken in order to design controllers. Later, the real time-varying parameter, r_L, will be taken into account.

The averaged load resistance R_L is given by

$$R_L \triangleq \frac{1}{t_f - t_0}\int_{t_0}^{t_f} r_L dt. \quad (7)$$

where t_0 and t_f are the initial and final time, respectively, in the rising transient period. Assume that R_L has the same value in the falling transient period.

A. Electrical model for control design

The general discrete DVS converter control problem in portable electronic systems are to obtain a high energy efficiency, small current peaks, fast transient periods and

[1] http://www.minalogic.com/

[2] Cortesy of Sylvain Miermont.

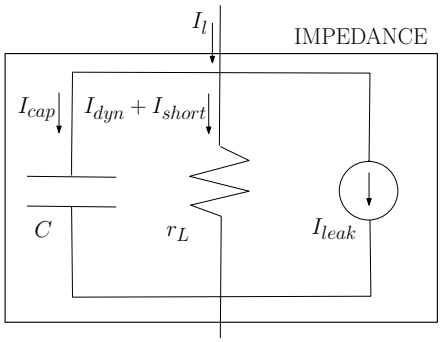

Fig. 2: Load model.

robustness and/or adaptation with respect to unknown electrical parameter.

For simplicity the low voltage supply, V_l, is disregarded for control design purposes (see Fig. 3). The main objective is that the core voltage v_c achieves the high and low voltage levels by switching the PMOS transistors. Note that, at least, one transistor must always be switched on.

Figure 3 shows an electrical representation of the DVS converter without the low voltage supply, V_l, connected to the load that has been described above.

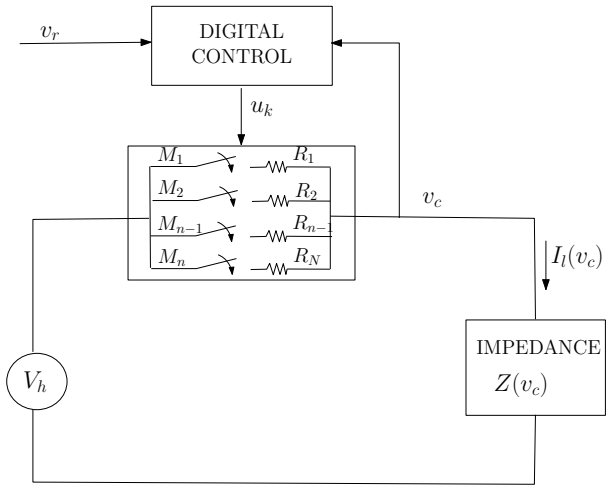

Fig. 3: Load with DVS converter without V_l.

Assume that the PMOS transistors are modeled as ideal resistors when they are switched on and, as resistors with infinite resistance when they are switched off. They are considered to have the same electrical characteristic.

The voltage loop equation yields the relationship

$$I_l(v_c) = \frac{V_h - v_c}{R_{u_k}}, \quad \text{where} \quad R_{u_k} \triangleq \frac{R_0}{u_k}. \tag{8}$$

u_k is the number of transistors switched on, thus, $u_k \in \mathcal{U} = \{1, 2, ..N\}$ and it will be the control variable. Likewise, R_0 is the PMOS transistor resistance.

Combining the specific form of the load, Eqs. (1)–(5), Eq.(6) and Eq. (7) with system (8), the voltage equation can be expressed as:

$$\dot{v}_c = -\beta v_c + b(V_h - v_c)u_k - \delta, \tag{9}$$

where

- $\beta \triangleq \frac{1}{R_L C} > 0$ and $\delta \triangleq \frac{I_{leak}}{C} > 0$ depend on the load.
- $b \triangleq \frac{1}{R_0 C} > 0$.

Define the voltage error as: $e \triangleq v_r - v_c$, where v_r is a voltage reference. Thus, the associated error voltage equation is

$$\dot{e} = -(\beta + bu_k)e + (bu_k + \beta)v_r - bV_h u_k + \delta + \dot{v}_r. \tag{10}$$

III. Control law

The objective of this section is to present a high performance control law for the discrete DVS converter. This controller must fulfill the requirements mentioned before for the transient periods, i.e., when the output voltage is scaled from a low voltage level to a high voltage level (rising transient period) and from a high voltage level to a low voltage level (falling transient period). This controller is designed to provide stable behavior by using control methodology.

In the steady states, the maximum stable voltage achieved is $V_h - \Delta_h$ and the minimum stable voltage achieved is $V_l - \Delta_l$ where $\Delta_h, \Delta_l \in \mathbb{R}$ depend on several factors and are difficult to estimate. These variables catch the PMOS model errors, current variations, supply voltage and the resistive losses through the PMOS transistors switched on.

Assumption 1: Δ_h, Δ_l are small with respect to v_c, and they do not change the system stability properties.

Some simulations are performed in such a way that the behavior of the closed-loop system with the different controllers are shown. In these simulations, $N = 24$ is taken as the total number of PMOS transistors in the model shown in Fig. 1. Note that at least, one active transistor must be always switched on. The voltage supply is $V_h = 1.2V$. The reference signal, v_r, is a step between the low voltage level $V_{c_l} = 0.8V - \epsilon_h$ and the high voltage level $V_{c_h} = 1.2 - \epsilon_h$, being $\epsilon_h = 0.06V$ and $\epsilon_l = 0.01$ ($V_{c_l} \approx V_l$). These parameters comes from the equilibrium of Eq. (10). This signal has a slope specified by the designer, which is inspired by [7].

The system resistances are $R_L = 39.67\Omega$ and $R_0 = 31.41\Omega$, the capacitance is $C = 9nF$ while $K_{leak} = 1.67 \cdot 10^{-3}$, the threshold voltage is $V_{th} = 0.4V$, and system frequency is $\omega_n = 500MHz$. The sampling frequency has the same value that the clock frequency. Finally, the slope of the reference signal, v_r, is $1.067 \cdot 10^6 V/s$.

A. Control proposed in [7]

The development of the high performance controller for the DVS converter is inspired by the 'intuitive control' used in [7], under the form:

$$u_k = \text{sat}_1^N\{u_{k-1} + \text{sign}(e)\}$$

In this law, no more than one transistor switches at each sampling time according to the sign of the voltage error. Therefore, this controller has the limitation that one only transistor can be switched on or off at every sampling

time. Figure 4 shows the implementation of this controller. Likewise, Fig. 5 shows a simulation for this controller by using Matlab. This controller is implemented in fixed-point by using 4 bits. Note that although this controller presents a simple implementation (only one addition), the performance presents an oscillatory behavior, with important current peaks.

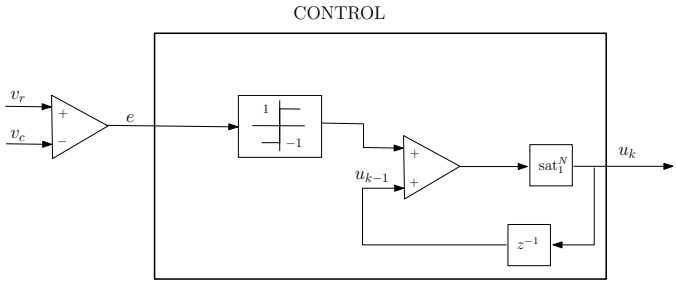

Fig. 4: Intuitive control from [7].

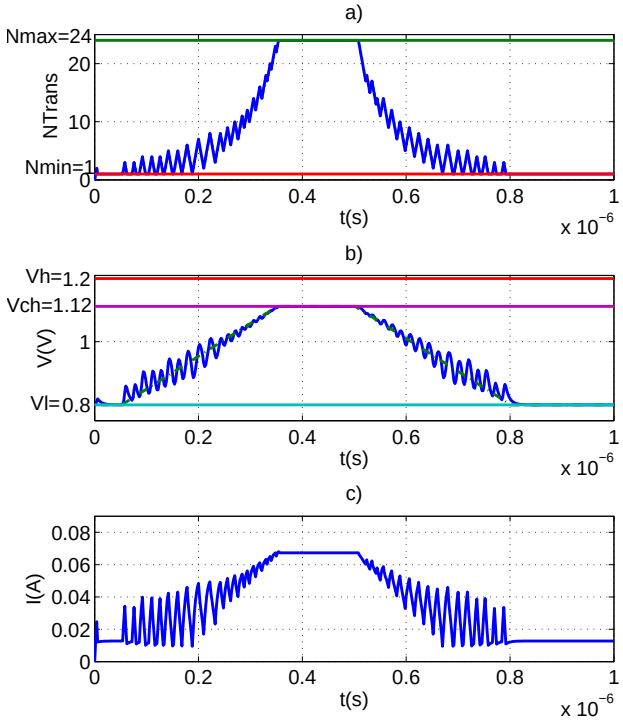

Fig. 5: Intuitive control. Evolution of the: a) number of PMOS transistors switched on, b) v_r (green) and v_c (blue), c) current. I_l.

In what follows, other control alternative is proposed without the limitation that only one transistor can be switched on or off, as long as the number of transistor is limited by 1 and N.

Remark 1: The control law is designed in such a way that the desired output voltage corresponds to one of the saturation bounds 1 or N, since they corresponds to the lower or higher voltage level, respectively.

The control law will be designed using directly the nonlinear continuous-time equation (10). This will lead to a continuous-time controller expression that will be approximately discretized. This approach is very common in the field of automatic control [13], [14]. The implementation of this discrete-time controller is shown by block diagrams.

The time evolution for the reference signal employed in [7] is maintained in the simulation of the developed controller in this section. However, later, it will be seen that, by means of choosing a suitable reference the closed-loop system performance can be enhanced.

B. Controller: Lyapunov-based design

The controller is designed guarantying closed-loop Lyapunov stability conditions for the equilibrium, $e = 0$. The design is performed employing the continuous-time error equation (10).

Consider the following Lyapunov function candidate

$$V_{lyap} = \frac{e^2}{2}.$$

Its time derivative is

$$\dot{V}_{lyap} = -\beta e^2 + (b(v_r - V_h)u_k - bu_k e + \beta v_r + \delta + \dot{v}_r)e. \quad (11)$$

The negativeness of $\dot{V}$ can be assured canceling the undesired terms. This can be performed by choosing

$$u_k = \frac{\beta v_r + \dot{v}_r + \delta}{b(V_h + e - v_r)}, \quad (12)$$

then Eq. (11) is

$$\dot{V}_{lyap} = -\beta e^2 \leq 0.$$

Therefore, $e = 0$ is asymptotically stable.

IV. Lyapunov control implementation

Now, the implementation of the Lyapunov controller is dealt with.

The approximate discrete-time version of Eq. (12) considering the saturation and rounding function for physical implementation purposes is:

$$u_k = \text{sat}_1^N \text{round}\left\{\frac{\beta T_s v_{r_k} + v_{r_k} - v_{r_{k-1}} + \delta T_s}{bT_s(V_h + e_k - v_{r_k})}\right\}$$

For implementation issues the division is remplaced by a multiplication for Φ.

$$u_k = \text{sat}_1^N \text{round}\left\{\left(K_1 v_{r_k} + K_2(v_{r_k} - v_{r_{k-1}}) + K_3\right)\Phi\right\} \quad (13)$$

where

- $K_1 \triangleq \frac{\beta T_s}{R_0}$,
- $K_2 \triangleq \frac{1}{R_0}$,
- $K_3 \triangleq \frac{\delta T_s}{R_0}$ and
- $\Phi \approx \frac{C}{T_s(V_h + e_k - v_{r_k})}$ takes the closest corresponding value to Table I.

This is the structure for the controller implementation.

v_{ck}	0.8	0.84	0.88	0.92	0.96
Φ	1.3	1.4	1.6	1.8	2.1
v_{ck}	1.0	1.04	1.08	1.12	
Φ	2.5	3.1	4.2	6.2	

TABLE I: Stored values of $\frac{C}{T_s(V_h+e_k-v_{r_k})}$.

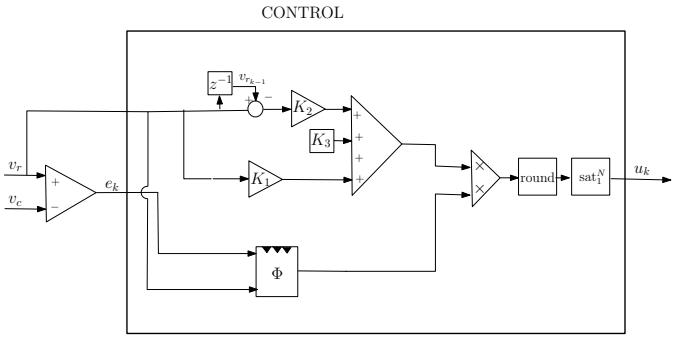

Fig. 6: Digital Lyapunov control.

Figure 6 shows a block diagram of this approximate discrete-time version. Note that it presents 3 additions/sustrations, 3 multiplications and an access table.

The performance of this controller is shown by simulation in Fig. 7. This controller is implemented in fixed-point by using 4 bits. Note that the application of this controller to the DVS converter reduces the current peaks, obtaining smoother voltage and current evolutions. However, the controller implementation presents some more operations than the 'intuitive controller'.

V. Performance evaluation

In this section a performance evaluation is performed for the resulting voltage and current signals in the transient period, after applying the previous controller. The voltage signal performance is evaluated by computing the mean and variance of the voltage error. Likewise, the current signal performance is evaluated by computing the maximum current peaks as well as its Power Spectral Density (PSD). This PSD is computed using all the recorded data, since this decompositions is computed after the simulation. These computations have been performed by Matlab.

Table II presents the mean and variance of the voltage error signal and maximum peak of the current signal.

	Mean Error	Var. Error	Max. Curr. Peak
Intuitive c.	$3.32 \cdot 10^{-3}$	$6.59 \cdot 10^{-5}$	$4.0 \cdot 10^{-2}$
Lyapunov c.	$2.24 \cdot 10^{-3}$	$3.37 \cdot 10^{-5}$	$0.5 \cdot 10^{-2}$

TABLE II: Performance evaluation.

Note that the new proposed controller improves the system performance with respect to the solution given in [7]. Observe that Lyapunov controller provides a PSD smaller than the 'intuitive controller' (Fig. 9 and 8).

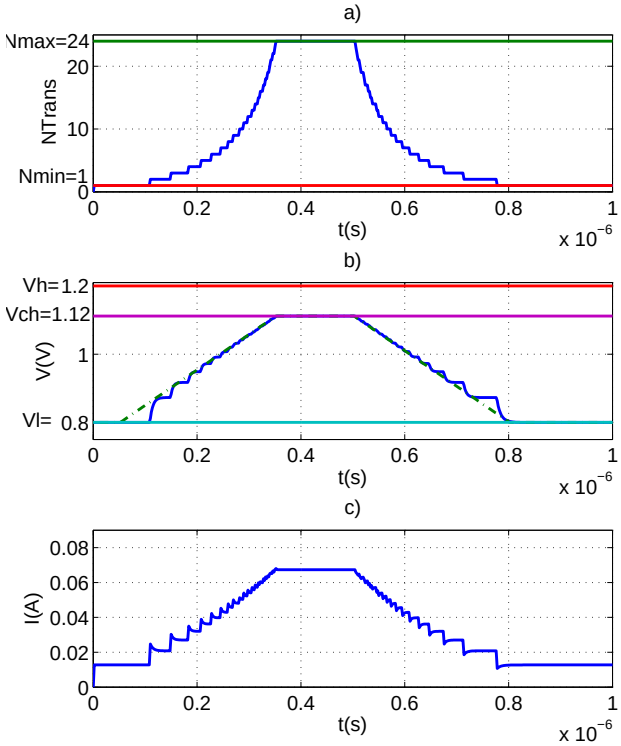

Fig. 7: Lyapunov controller. Evolution of: a) number of PMOS transistors switched on, b) the v_r (green) and evolution of v_c (blue) and c) the current I_l.

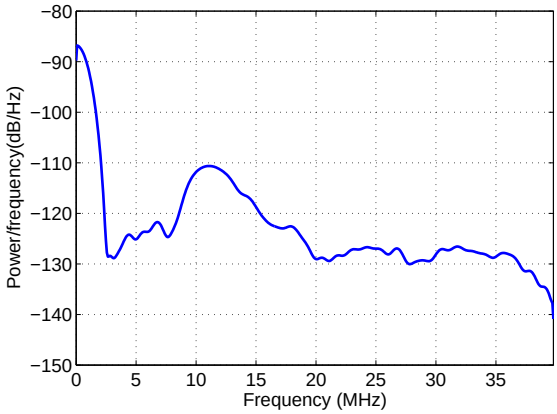

Fig. 8: Power spectral density with 'intuitive controller'.

A. Cost performance

Concerning to implementation issues, note that the 'intuitive controller' presents a simpler implementation than the Lyapunov controller. Table V summarizes the numerical operations and the bits needed for the implementation of theses controllers.

Note that the Lyapunov controller generates a better performance in spite of introducing more numerical operations. However, the number of bits are maintained in fixed-point implementation.

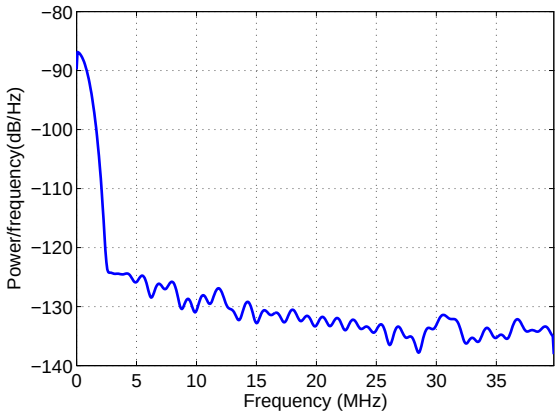

Fig. 9: Power spectral density with Lyapunov controller

	Addit	Multipl.	Acc. table	bits
Intuitive control	1	0	0	4
Lyapunov control	3	3	1	4

TABLE III: Implementation cost.

B. Energy evaluation

In the set of PMOS, the accumulated dissipated energy in the transient period depends on the control law employed, i.e., on the switching sequence. For instance, undesirable oscillatory current profile can be obtained with certain controllers. This non-smooth behavior of the transient current may result in a higher energy consumption. The purpose here is to evaluate the energy cost during the transient periods associated with the controller presented in previous section.

The ideal dissipated energy in the PMOS transistors during the transient period is

$$E_d = \int_{t_0}^{t_f} (V_h - v_c) I_l dt$$

where t_0 is the initial time and t_f is the final time in such transient period. Figure 10 and Table IV show the dissipated energy during the rising transient period.

Note that the energy consumption obtained with the Lyapunov controller is improved with respect to the 'intuitive controller'. This is due to the smoother behavior of voltage and current signals obtained with this controller.

	Dissip. Total Energy (μJ)
Intuitive control	7.2
Lyapunov control	4.8

TABLE IV: Dissipated total energy in rising transient period.

C. Summary

The intuitive control proposed in [7] provides a reasonable tracking at the expense of an oscillatory behavior due to its own limitation. This involves that the current signal time profile presents a high frequency behavior with some

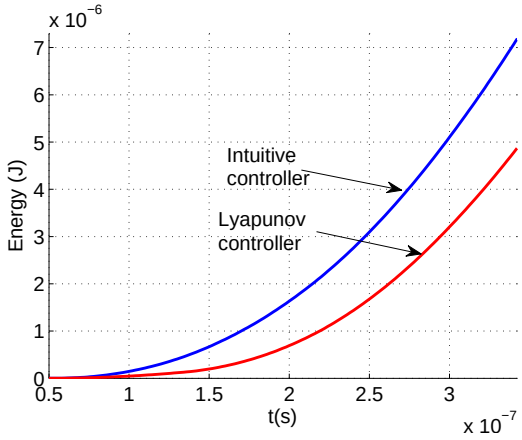

Fig. 10: Energy dissipated during the rising transient period with the 'intuitive controller' and the Lyapunov.

substantial peaks, in particular when the total PMOS parallel resistances are larger. This seems to be the main cause of larger dissipated energy.

The highlight of Lyapunov's controller is its energy consumption reduction, which is due to the smoother behavior of the voltage and current time profiles. This involves that the controller reduces by 32% the energy consumption with respect to the 'intuitive control'. On the other side, the number of bits required for fixed-point implementation is maintened. Its higher number of operations is affordable in this application. It supposes a minimum cost in comparison with the favorable performance.

The presented advantages became essential in nanoelectronic technology. However, other improvements are accomplished to obtain an even higher performance.

VI. Advanced Lyapunov's controller

The Lyapunov's controller (Eq. (12)) presents very suited properties for the DVS converter. However, this controller can be improved.

Firstly, minimum energy consumption and current peaks are desired. This can be achieved finding an appropriate evolution for the voltage reference, $v_c^*(t)$, by applying optimal control theory [16], [15], [17].

Secondly, note that the Lyapunov's controller depends on the resistance load parameter, β. However, this parameter is, in many occasions, difficult to estimate and may change with time, as mentioned in Section II. Therefore, a second objective is to design an adaptation law in order to obtain an estimation $\hat{\beta}$ for the unknown parameter.

The proposed control architecture including the optimal reference and the adaptation mechanism is shown in Fig. 11.

VII. Optimal voltage reference computation

Assume that the desired voltage is constant. The problem may be formulated as to find a continuous-time voltage reference trajectory from a voltage initial value $v_c(t_0)$ to set-point v_r, minimizing current peaks, ΔI, and the

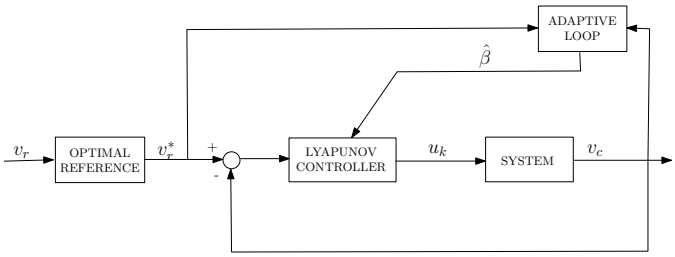

Fig. 11: DVS converter closed-loop with optimal evolution of the voltage reference and adaptation parameter.

dissipated energy. This problem will be addressed applying continuous-time optimal control theory [16], [15], [17].

In order to optimize the current peaks, time derivative of the current $\dot{I}_l$ is included in the performance index. In every sampling time, a certain number of transistors will be switched on. The total number of PMOS transistors switched on at the previous sampling time is denoted by u_k^-, and the total number of PMOS transistors switched on at the current sampling time is denoted by u_k^+. Consequently, the number of PMOS transistors switched on or off in every sampling time is given by $\Delta u_k = u_k^+ - u_k^-$.

The current peaks are due to the sudden change of the PMOS resistance at the sampling times. These peaks $\Delta I_l = I_l^+ - I_l^-$ are given by

$$\Delta I_l = \frac{V_h - v_c}{R_0}(u_k^+ - u_k^-) = \frac{V_h - v_c}{R_0}\Delta u_k.$$

The same notation given above for u_k^+ and u_k^- is used here for variable I_l. Therefore, the continuous-time approximation for the current peaks is

$$\dot{I}_l \approx \frac{V_h - v_c}{R_0}\dot{u}.$$

Another way to achieve this same expression is taking time derivative of I_l given by Eq. (8). Rigorously, the time derivative of this current is

$$\dot{I}_l = \frac{V_h - v_c}{R_0}\dot{u} - \frac{\dot{v}_c}{R_0}u.$$

Nevertheless, it can be seen by simulation that during a typical transient period, the last term is very small (see Fig. 12). This simulation is performed using the same parameters given in Section III. This graph supports the previous argument.

Consider the following performance index

$$J = \int_0^\tau L(e, u, t)dt, \tag{14}$$

where the final time τ is free and the Lagrangian $L(e, u, t)$ is chosen in order to penalize:

- voltage error e,
- dissipated power $P = (V_h - v_c)I_l$ and
- current peaks $\dot{I}_l$.

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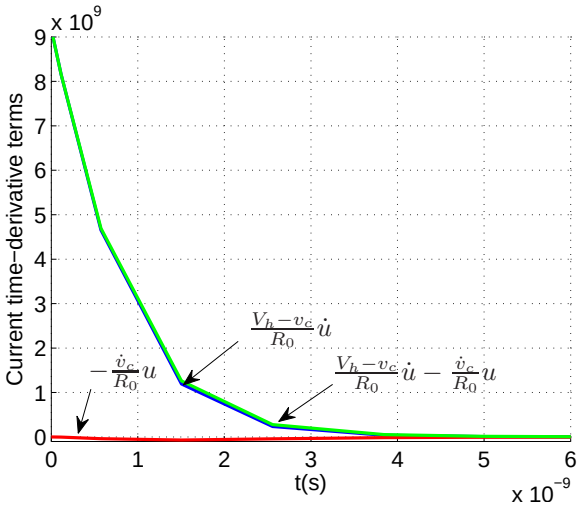

Fig. 12: Current time-derivative terms.

The following Lagrangian is chosen

$$L = q_1 e^2 + q_2\left(\frac{(V_h - v_r + e)^2}{R_0}u\right)^2 + \left(\frac{V_h - v_r + e}{R_0}\dot{u}\right)^2, \tag{15}$$

where q_1 and q_2 are positive weighting constants. The first term of Eq. (15) penalizes the voltage error, the second one penalizes the dissipated power and the last one, the current peaks.

Consider a 2-dimensional optimal control problem $x = [e, u]$ with $\dot{x} = [\dot{e}, \nu]$, where $\nu \triangleq \dot{u}$. Thus, the Hamiltonian function is

$$H = q_1 e^2 + q_2\frac{(V_h - v_r + e)^4 u^2}{R_0^2} + \frac{(V_h - v_r + e)^2\nu^2}{R_0^2} + \lambda_1[b(-V_h + v_r - e)u + \beta + \delta] + \lambda_2\nu. \tag{16}$$

Solving the algebraic equation

$$\left.\frac{\partial H(e, \nu, \lambda_1, \lambda_2)}{\partial \nu}\right|_{\nu=\nu^*} = 0,$$

the optimal $\nu^*(x, \lambda)$ is

$$\nu^* = \frac{-\lambda_2}{2}\left(\frac{R_0}{V_h - v_r + e}\right)^2$$

which gives the optimal Hamiltonian expression

$$H^*(e, \lambda_1, \lambda_2) = q_1 e^2 + q_2\frac{(V_h - v_r + e)^4 u^2}{R_0^2} - \frac{\lambda_2^2 R_0^2}{2(V_h - v_r + e)^2} + \lambda_1[b(v_r - V_h - e)u + \beta + \delta]. \tag{17}$$

The optimal solution is associated with the set of differ-

ential equations:

$$\frac{\partial H^*}{\partial \lambda_1} = b(v_r - V_h - e)u + \beta + \delta = \dot{e} \quad (18)$$

$$\frac{\partial H^*}{\partial \lambda_2} = \frac{-\lambda_2}{2}\left(\frac{R_0}{V_h - v_r + e}\right)^2 = \dot{u} = \nu \quad (19)$$

$$\frac{\partial H^*}{\partial e} = 4q_2\frac{(V_h - v_r + e)^3}{R_0^2}u^2 + \frac{(\lambda_2 R_0)^2}{2(V_h - v_r + e)^3} + 2q_1 e + -bu\lambda_1 - \beta\lambda_1 = -\dot{\lambda}_1 \quad (20)$$

$$\frac{\partial H^*}{\partial u} = \frac{2q_2 u(V_h - v_r + e)^4}{R_0^2} + b\lambda_1(v_r - V_h - e) = -\dot{\lambda}_2 \quad (21)$$

with the boundary conditions,

$$e(0) = v_r - v_c(0) \quad (22)$$

$$e(\tau) = 0 \quad (23)$$

$$u(0) = \text{PMOS transistors switched on in } t = 0 \quad (24)$$

$$u(\tau) = \text{PMOS transistors switched on in } t = \tau \quad (25)$$

and, the transversality condition

$$H^*(\tau) = 0. \quad (26)$$

Note that this is a nonlinear Boundary Value Problem (BVP) with a transversality condition, since the final time τ is unknown.

Solving (18)–(26) yields e^*, from which, the optimal voltage evolution $v^* = v_r - e^*$ can be derived. This evolution can be employed as reference for the controllers developed in Section III.

A. Numerical solution

The problem raised before: finding a solution for (18)–(26) with (22)–(25) and (26), is a complex problem because it is a nonlinear BVP with a four dimensional character and it has a transversality condition. A numerical solution is proposed. Nevertheless, finding this numerical solution is also an involved task. There is not so many tools that cope with this kind of problems. In this case the Matlab function 'bvp4c' has been employed. Function bvp4c [9] combines the solution of Initial Value Problem (IVP) for Ordinary Differential Equations (ODEs) and the solution of algebraic equations, being a non-shooting code. The nonlinear algebraic equations are solved iteratively by linearization, providing a suited initial guess after some iterations over a mesh and taking into account the boundary conditions. This is due to the fact that can have more than one solution and, thus, a guess for the desired solution must be provided by designers, which includes an initial mesh for this desired solution.

Function bvp4c controls the error of the numerical solution and adapts the mesh in every iteration to obtain an accurate numerical solution with a modest number of mesh points. Thus, obtaining a 'residual' error is common. If the residual error is small, then the solution provided by function bvp4c is a suited solution.

Function bvp4c is not directly applicable for the present problem since it cannot handle the transversality condition. Thus, this function has been used iteratively in order to obtain a solution that fulfills condition (26). The system parameters given in Section III are reported. Furthermore, it is only considered the rising transient period, i.e, when output voltage goes from the low voltage level to the high voltage level. Therefore, the next boundary conditions are selected:

$$e(0) = v_r - v_c(0) \quad (27)$$

$$e(\tau) = 0 \quad (28)$$

$$u(0) = 1 \quad (29)$$

$$u(\tau) = N \quad (30)$$

The following values for the weighting constants are chosen[3],

$$q_1 = 0.64 \quad (31)$$

$$q_2 = 0.32. \quad (32)$$

Using as initial guess

$$e(t) = 0.3e^{-10^8 t}$$
$$u(t) = 24 - 23e^{-10^8 t}$$
$$\lambda_1(t) = 10^6 t + 10^5$$
$$\lambda_2(t) = -3.2 \cdot 10^7 t^2 - 3.2 \cdot 10^7 t + 100,$$

Note that this initial guess has a complex form and, thus, it has been difficult to obtain. As mentioned before, this is a complex problem, and finding a solution has been very involved. However, with the future numerical methods, it is expected that new tools for this kind of problem will be researched and developed.

The nonlinear BVP (18)–(21) with the specified boundary conditions (27)–(30) reaches the numerical solution shown in Fig. 13. Note that, the boundary conditions in e^* and u^* are satisfied when $\tau = 23.3 \cdot 10^{-9} s$. From e^*, the optimal voltage reference v^* can be obtained.

Figure 14 shows the evolution of H^*, whose value at $\tau = 23.3 \cdot 10^{-9} s$ is close to zero, fulfilling the transversality condition.

Observe that, this voltage reference has been computed for the rising transient period. For the falling transient period, a similar procedure can be applied.

VIII. Adaptive feedback control design

The Lyapunov's controller (Section III) has been designed under the assumption that the parameter β is known. In this section, an adaptive law is proposed in order to cope with the case when the load parameter β is unknown or/and changes slowly.

Denote $\hat{\beta}$ as the estimated value for the load parameter. This estimated parameter will be used in control law (12) instead of the real value,

$$u_k = \frac{\hat{\beta} v_r + \dot{v}_r + \delta}{b(V_h + e - v_r)}, \quad (33)$$

[3]As usual in optimal control problems, they have been chosen in a trial-and-error procedure, checking by simulations the solutions obtained.

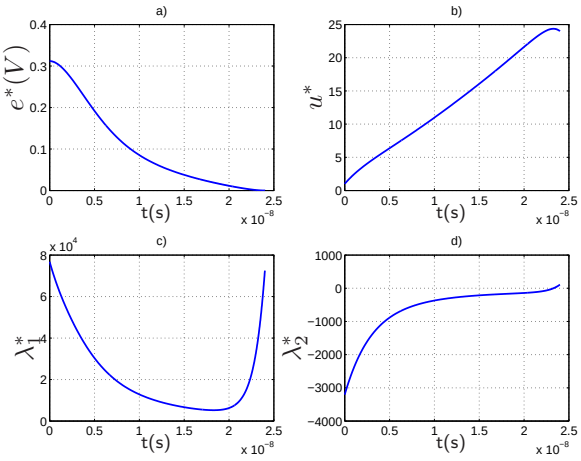

Fig. 13: Optimal numerical solution. a) error evolution, b) control evolution, c) λ_1 evolution and d) λ_2 evolution.

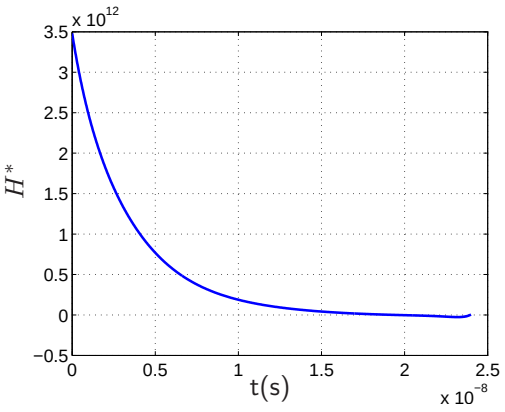

Fig. 14: H^* evolution.

Now, the closed-loop system of (10) with controller (33) yields

$$\dot{e} = -\beta e + \beta v_r - \hat{\beta} v_r. \tag{34}$$

Assume that β is a constant parameter which involves $\dot{\beta} = 0$ and define

$$\tilde{\beta} = \beta - \hat{\beta}, \quad \dot{\tilde{\beta}} = -\dot{\hat{\beta}}.$$

For the adaptive control system, the next Lyapunov function candidate is proposed

$$W = \frac{e^2}{2} + \frac{\tilde{\beta}^2}{2\gamma}, \tag{35}$$

where γ is a positive design parameter that may define the adaptation speed.

Differentiating W with respect to time, yields

$$\dot{W} = -\beta e^2 + \tilde{\beta}\left(v_r e + \frac{\dot{\tilde{\beta}}}{\gamma}\right).$$

Note that $\beta > 0$, as has been seen above. The adaptive law is designed by canceling the term in brackets, i.e.:

$$\dot{\hat{\beta}} = -\dot{\tilde{\beta}} = \gamma v_r e. \tag{36}$$

This achieves $\dot{W} = -\beta e^2$.

Asymptotic stability is established by LaSalle's invariance principle [18]. Consider the level set $W_c = W(e, \tilde{\beta}) \leq c_0$ for sufficiently large $c_0 > 0$, where $\dot{W} \leq 0$. This set is compact and positively invariant.

Note that $\dot{W} = 0$ on $e = 0$. Furthermore, note from Eq. (34), that

$$e(t) \equiv 0 \quad \Rightarrow \quad \dot{e}(t) \equiv 0 \quad \Rightarrow \quad \tilde{\beta}(t) \equiv 0.$$

Therefore, the maximum invariant set in W_c with $\dot{W} = 0$ corresponds to the single point $P_1 = (e = 0, \tilde{\beta} = 0)$, thus, every solution starting in W_c approaches the desired point P_1 as $t \to \infty$.

IX. Evaluation of the advanced Lyapunov's controller

In this section, an evaluation of the advanced Lyapunov controller with respect to performance cost and energy saving is performed by doing some simulations.

The resulting controller (13) after applying the optimal voltage reference and the adaptive law is

$$u_k = \text{sat}_1^N \text{round}\left\{\left(\bar{K}_1 \hat{\beta} v^*_{r_k} + K_2(v^*_{r_k} - v^*_{r_{k-1}}) + K_3\right)\Phi\right\} \tag{37}$$

where $v^*_{r_k}$ and $v^*_{r_{k-1}}$ comes from the discretization of the optimal voltage reference, which has been previously obtained. For implementation, the values of $v^*_{r_k}$ can be stored in a table. In the same way, $\bar{K}_1 \triangleq \frac{T_s}{R_0}$ and $\hat{\beta}$ is adapted by the discrete-time approximation of the adaptation law (36):

$$\tilde{\beta}_k = \tilde{\beta}_{k-1} - K_4 v^*_{r_k} e_k$$

where $K_4 \triangleq T_s \gamma_1$.

Some simulations of this controller in the DVS converter are performed by using the data reported in Section III. In order to perform more realistic tests, a more precise model for the load is considered in such a way that β depends on r_L, i.e., it is time-varying. The bounds on β are: $\beta_{min} = 1.38 \cdot 10^7$ for $v_c = V_l$ and $\beta_{max} = 5.9 \cdot 10^7$ for $v_c = V_h$. As initial estimated values is taken $\hat{\beta} = 0$.

Figure 15 shows the closed-loop performance by employing the optimal voltage reference and the adaptation mechanism. Note that when the adaptation mechanism is implemented the system can achieve a similar performance to the case of known load. Although, the adaptive control introduces a delay in the system response, small current peaks and faster transient periods are obtained. This simulation were performed in fixed-point by using 4 bits.

The adaptation of the load resistive component β is shown in Fig. 16. Note that β approaches its real value, in spite of the fact that β is time-varying. Observe that the time-evolutions of $\hat{\beta}$ and β are superimposed.

A. Performance cost

Note that the adaptive controller increases the number of numerical operations. Table V summarizes the numerical operations and the bits that need the controllers presented in this paper.

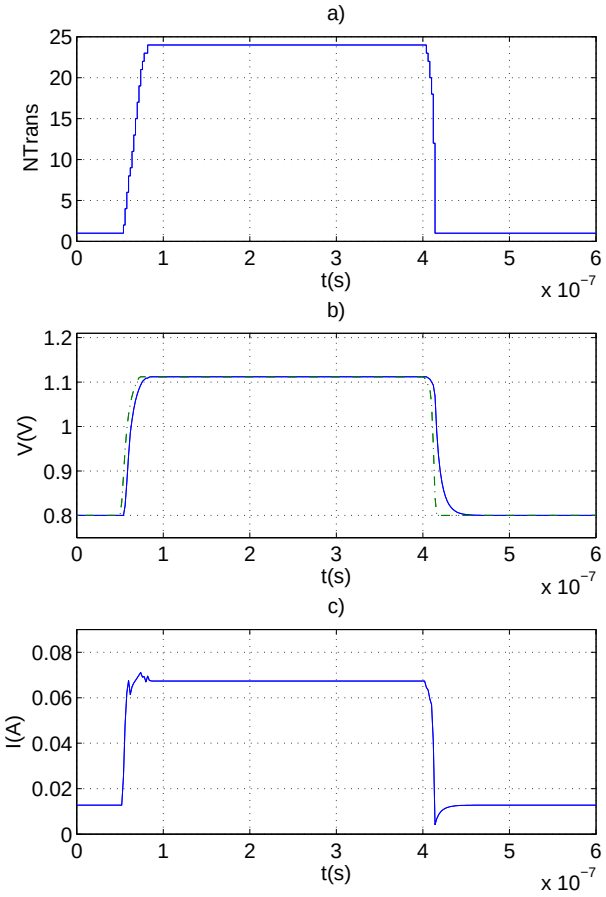

Fig. 15: DVS converter with the advanced Lyapunov controller and adaptation $\hat{\beta}$. Evolution of a) number of PMOS transistors switched on, b) v_r (green) and v_c (blue) and c) current I_l.

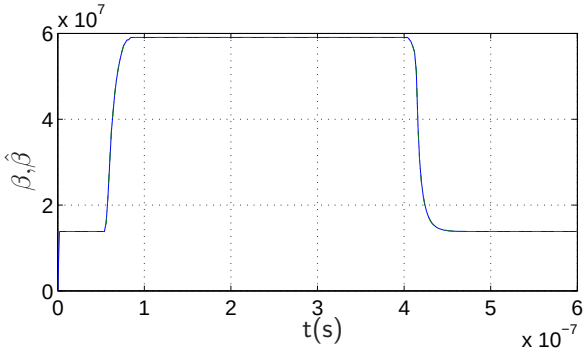

Fig. 16: Time-evolution of $\hat{\beta}$ (blue) and β (green) by using the advanced Lyapunov controller.

	Addit	Multipl.	Acc. table	bits
Intuitive control	1	0	0	4
Lyapunov control	3	3	1	4
Adv. Lyap. control	4	6	1	4

TABLE V: Implementation cost.

Note that this controller needs the same number of bits for fixed-point implementation. The number of numerical operation is affordable for SoC integration. Although the advanced Lyapunov controller implementation is higher, its performance is optimal: shorter transient period, minimum current peaks and load variability adaptation.

B. Energy evaluation

Another effect of the obtained voltage reference is the reduction of the energy consumption, as is shown in Fig. 17. The accumulated dissipated energy in the rising transient period is summarized in Table VI. The energy saving with respect to the 'intuitive controller' is 93%. Likewise, the transient period is reduced to $23.3ns$.

	Dissip. Total Energy (μJ)
Intuitive control	7.2
Lyapunov control	4.8
Advanced Lyapunov control	0.5

TABLE VI: Dissipated total energy in rising transient period.

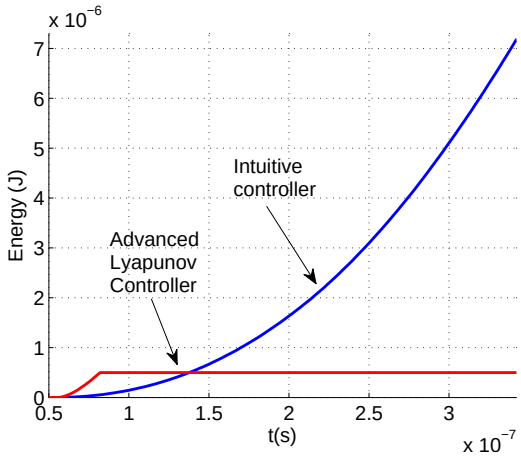

Fig. 17: Dissipated energy in the rising transition.

Consequently, the reliability and efficiency of the advanced Lyapunov controller, which uses the optimal voltage reference and the adaptation mechanism, has been validated. Besides, the fact, that there exists a time-varying load parameter is not relevant for the right system performance. In addition, this controller has an important energy dissipation reduction as well as small current peaks and fast transient periods. And its implementation cost is affordable.

C. Simulations using a more accurate model

In this paper, some assumptions have been formulated. These assumptions allow to obtain a model that is simple enough and is not more complicate than necessary for the DVS converter. From this model, a control structure with a moderate complexity and dimension should be developed. However, there obviously are unmodeled components that could make the control methods developed here invalid. For this reason, in this section a robustness analysis is performed with a more real DVS model.

In section II, it was considered that all transistors are modeled as an ideal resistance when they are switched on. Now, it is considered that the transistor models are composed by a resistance and a capacitance, in order to model the dissipative effects as well as the switching periods of the PMOS transistors. Moreover, the transistors have different electrical characteristics. On the other side, it is considered that the sensor that measures the core voltage, v_c, is modeled as a low-pass filter. These new characteristics are shown in Fig. 18.

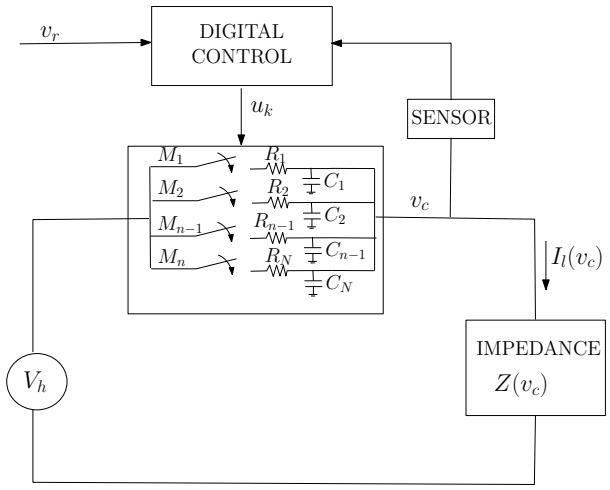

Fig. 18: A more real model of the DVS converter.

The system is now modeled as

$$I_l(v_c) = (V_h - v_c)\sum_{i=1}^{u_k}\frac{1}{R_i} + \sum_{i=1}^{u_k} C_i\frac{dv_c}{dt}, \qquad (38)$$

where $R_i \in [25, \quad 37]\Omega$, and $C_i \in [1, \quad 5]\cdot 10^{-10}$F. Note that, the system response of this more accurate model with the advanced Lyapunov controller developed in this paper provides a robust behavior.

Figure (19)–(20) show some simulations of (1)–(6) and (38) where R_i and C_i ware assigned random values in the ranges $25 \leq R_i \leq 37$ and $10^{-10} \leq C_i \leq 5\cdot 10^{-10}$. In these simulations, it is considered that the voltage sensor presents a response time of 10^{-8}s.

X. Conclusion

In this work, a Lyapunov controller has been designed for a DVS converter. This controller improves the performance over the one used in [7] in terms of transient

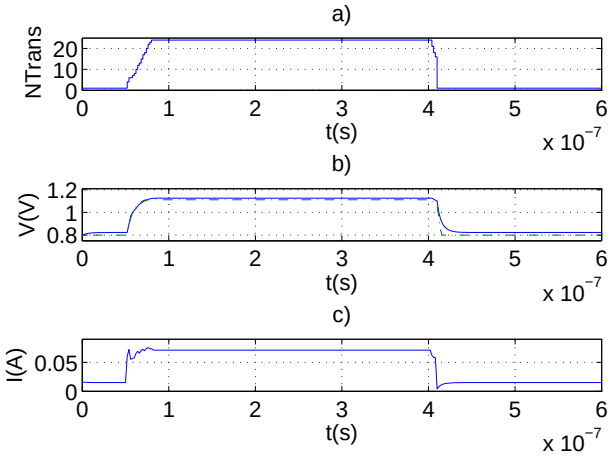

Fig. 19: DVS model (38) with R_i and C_i random values, load (1)–(6) and advanced Lyapunov controller.

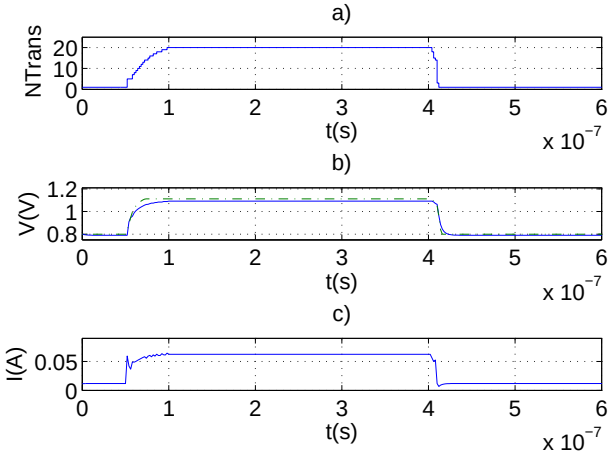

Fig. 20: DVS model (38) with R_i and C_i random values, load (1)–(6) and advanced Lyapunov controller.

response, as mentioned in Section V. This controller is a very simple controller with a strong limitation: only one transistor can be switched on or off in every sampling time. The good results obtained with the controller developed in this paper comes from applying control theory as well as the possibility to let such controller to switch more than one transistor at once.

In a performance evaluation presented in Section V to the Lyapunov controller, it has been concluded that this controller offers a suited performance, from of point of view of the current peaks and energy consumption. Nevertheless, this controller can be enhanced, if both optimal and adaptive control are developed. These control approaches allow to diminish energy consumption and current peaks and deal with unknown load resistive parameter, respectively. A robustness analysis shows the controller reliability when it is applied to a more accurate model.

The contribution highlights obtained with the advanced Lyapunov controller developed here are:

1) Energy saving: A method to obtain an optimal reference has been developed applying optimal control theory [16], [15], [17]. However, the problem stated for this method presents a high complexity, because it is a BVP with transversally condition for a 4^{th}-order optimal problem. This numerical solution has been obtained by employing the Matlab function bvp4c. It has been a involved task, and it is expected that new mathematic tools will be developed to make easier to compute this voltage reference. This result achieves a reduction of current peaks and 90% energy saving with respect to the previous Lyapunov controller. This fact makes that the total energy saving with respect to the 'intuitive controller' used in [7] is 93% reduction.

2) Adaptation to parameter variability: In addition, an adaptive strategy is developed in order to deal with the load modeling error. Moreover, in order to prove the reliability of this adaptive controller, it has been introduced by simulation that parameter β is time-varying, as is common in practice.

3) Affordable performance cost: The suited performance resulting of applying the advanced Lyapunov controller in the DVS converter has been shown in fixed-point simulation by using 4 bits. The implementation and the performance cost are affordable.

4) Circuit/control co-design: Control theory can help to improve the electronic design of the DVS system, as improved, in this paper, the original reference signal implemented for the DVS converter in [7]. In addition, in the paper, it is assumed that there exists a known number of PMOS transistors with the same electrical characteristic. By means of using control theory (as a design tool), it is possible to design a reduced number of non-homogeneous transistors (i.e. different resistance values) yielding similar closed-loop performance. The advantage is that the total number of PMOS transistors can be reduced.

In summary, a high-performance controller which does not need knowledge of the load resistive parameter has been obtained. This controller reduces energy consumption as well as current peaks, and transient periods. Its implementation is affordable and this study can improve the circuit design. These can enhance the future SoC miniaturization processes.

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